D. Remarks

Rejection of Claims 1, 2, 7, 8 and 13 Under 35 U.S.C. §102(b) based on U.S. Patent No. 5,329,139 (*Sanada*).

The rejection of claims 1 and 2 will first be addressed.

The invention of amended claim 1 recites a semiconductor apparatus that includes a plurality of device elements formed on a surface of a semiconductor substrate, each device element having a diffusion region. A multi-layer wiring configuration electrically connecting at least two of the diffusion regions, the multi-layer wiring configuration containing a plurality of wiring layers. A first one of the plurality of wiring layers is divided into a first wiring region for providing wiring in a first direction and a second wiring region for providing wiring in a second direction. In addition, predetermined wiring in the first one of the plurality of wiring layers is electrically connected to and disposed in parallel with wiring in a second one of the plurality of wiring layers.

As is well known, a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single reference.

The portion of *Sanada* relied upon in the rejection is not believed to show a wiring of a first wiring layer that is connected to, and disposed in parallel with, a wiring of a second wiring layer. Figure 7 of *Sanada*, relied upon by the rejection, shows an output signal line 34d (argued to correspond to Applicant's first wiring layer) that is electrically connected to a standardized wiring strip 34e (argued to correspond to Applicant's second wiring layer). However, in the arrangement shown, such wirings are perpendicular to one another, and not parallel, as recited in claim 1.[1]

Thus, because the rejection does not appear show parallel arranged wirings as recited in claim 1, this ground for rejection is traversed.

The rejection of claims 7, 8 and 13 will now be addressed.

The semiconductor apparatus of amended claim 7 includes a plurality of functional circuit blocks disposed in a matrix on the surface of a semiconductor substrate. Each functional circuit

[1] See *Sanada*, FIG. 7, which shows output signal line 34d that is perpendicular to standardized wiring strip 34e.

block including a plurality of device elements, a first wiring region and a second wiring region. Also included is a multi-layer wiring configuration electrically connecting predetermined ones of the device elements. A first one of the plurality of wiring layers is divided into a first wiring region for providing wiring in a first direction and a second wiring region for providing wiring in a second direction.

The portion of *Sanada* relied upon in the rejection is not believed to show functional circuit blocks disposed in a matrix on the surface of a semiconductor substrate. Figure 7 of *Sanada*, relied upon by the rejection, shows a single inverter circuit, and not a matrix of circuit blocks, as recited in claim 7.[2]

Thus, because the rejection does not appear show all limitations of claim 7, this ground for rejection is traversed.

Claims 1, 3, and 7 have been amended. The present claims 1-13 are believed to be in allowable form. It is respectfully requested that the application be forwarded for allowance and issue.

Respectfully Submitted,

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[2] See *Sanada*, FIG. 7, and description at Col. 5, Lines 65-68, which indicate the circuit is a complementary inverter.